AIAD #10860

Research Opportunity (1 faculty, and optionally 1-3 cadets)

ORGANIZATION/PROJECT SPONSOR
Organization: US Army Research Lab, SEDD (RDRL-SES-P)
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Location of Sponsoring Directorate or Division (City, State) Adelphi, MD

PROJECT Title: Ultra-low SWaP processing for Electric-field sensing applications

Description: Electric-field sensors, operating at frequencies in the audio band, have recently been used in field experiments to detect and characterize electric power activity, and also bullets in flight. Prototype algorithms have been developed in Matlab. There is a need to mature this technology by designing and building processing hardware with ultra-low size, weight, and power (SWaP). A PIC-class (~1 mW) microcontroller is envisioned, but other architectures should be investigated in light of algorithm issues and SWaP considerations before selection.

ARL/Army Benefit: ARL would be able to transition new technology to soldiers more quickly; ARL would develop a collaborative relationship with USMA in a new technology area.

Backgroud Required: The faculty should have experience with low-power, audio-frequency digital circuit design (including circuit analysis software, PCB layout tools), and also algorithm porting issues (from Matlab). The first 1-2 cadets should have experience with microprocessor and/or DSP-based programming. The third cadet should have experience with Matlab programming and basic statistical analysis.

Security clearance required: Secret clearances are strongly preferred; however, it may be possible to work with a cadet (US citizen with a NAC) but no clearance.

Capacity: (maximum number of faculty/cadets you would like working on this project): Recommend one faculty, and optionally 1-3 cadets. The faculty can oversee the project (primary daily interface with cadets), address hardware architecture and algorithm porting issues, and be primarily responsible for PCB design, layout, and testing. One cadet could be assigned to port each of two very different algorithms from Matlab to the selected DSP architecture. Another cadet project would involve characterizing signatures of many different pieces of equipment, and developing a library of reference signatures that can be used by one of the algorithms.

Duration: 6-12 weeks (with options for project extensions)

Block Preference: None